Georgios Vavouliotis

✉ gvavou5@gmail.com • 🌐 gvavou5.github.io • in georgios-vavouliotis

Research Interests

Computer Architecture, High Performance Computing, Machine Learning for Computer Architecture, Data Centers; identifying and exploiting the predictability of programs to design μarchitectural prefetching and prediction mechanisms for the cache and the TLB hierarchy, improving cache/TLB management for emerging applications with large data and code footprints, leveraging machine learning algorithms to design intelligent μarchitectural components, and re-thinking μarchitectural designs for server and data center applications.

Education

Universitat Politècnica de Catalunya (UPC) — Barcelona
Doctor of Philosophy (Ph.D.), Advisors: Dr. Marc Casas, Dr. Lluc Alvarez — Sept 2018-Dec 2022
Advanced Hardware Prefetching in Virtual Memory Systems (Cum Laude Award)

National Technical University of Athens (NTUA) — Athens
Diploma (M.Eng.) on Electrical & Computer Engineering (M.Sc. equivalent), **GPA: 8.9/10** — 2012-March 2018

Academic Directions
- *Computer Systems & Software*
- *Computer Networks and Networks Security*
- *Signal Processing, Automatic Control and Robotics*

Employment

Huawei Zurich Research Center — Zurich
Postdoctoral Researcher — Feb 2023–now

Huawei Zurich Research Center — Zurich
Research Internship — Nov 2021–April 2022
Impact of Concurrent Java Garbage Collectors on Cache Locality

Barcelona Supercomputing Center (BSC-CNS) — Barcelona
Researcher at Computer Architecture & Operating Systems Group — Sept 2018–Dec 2022

National Technical University of Athens (NTUA) — Athens
Research Student at Computer Systems Laboratory (CSLab) — Feb 2018–July 2018

Honors and Awards

Cum Laude Ph.D. Award — Spain
For my Ph.D. dissertation entitled Advanced Hardware Prefetching in Virtual Memory Systems — 2023

Hisilicon Core Star Award (awarded by Huawei) — Shenzhen
For the Concurrent GCs and Modern Java Workloads: A Cache Perspective paper — 2023

Best Paper Award - ISMM 2023 — Orlando
For the Concurrent GCs and Modern Java Workloads: A Cache Perspective paper — 2023

HiPEAC 2022 Paper Award — Chicago
For the Page Size Aware Cache Prefetching paper — 2022

Travel Grant for MICRO'22 — Chicago
MICRO 2022 Conference — 2022

Travel Grant for ISCA'22 — New York
ISCA 2022 Conference — 2022

HiPEAC 2021 Paper Award — Virtual
For the Morrigan: A Composite Instruction TLB Prefetcher paper — 2021

HiPEAC 2021 Paper Award — Virtual
For the Exploiting Page Table Locality for Agile TLB Prefetching paper — 2021

○ **Best Poster Award**   **Virtual**
2021 ACM School on HPC Computer Architectures for AI and Dedicated Applications   *2021*

○ **2019 FPI Doctoral Fellowship**   **Barcelona**
Funded by Spanish Government (MINECO)   *2019-2022*

○ **Travel Grant for ASPLOS'20**   **Lausanne/Virtual**
ASPLOS 2020 Conference   *2020*

○ **Mathematics Award - National Technical University of Athens (NTUA)**   **Athens**
Excellent marks in all mathematical courses during the first two (2) years.   *2014*

○ **"The Great Moment of Education" Eurobank EFG Scholarship**   **Chalkida**
Highest rank in National Qualifications Exams in my school   *2012*

Peer-Reviewed Conference Publications

[1] Alexandre Valentin Jamet, **Georgios Vavouliotis**, Lluc Alvarez, Daniel A. Jiménez, Marc Casas, Practically Tackling Memory Bottlenecks of Graph-Processing Workloads (to appear). Proceedings of the 38th IEEE International Parallel & Distributed Processing Symposium (IPDPS), San Francisco, May 2024.

[2] Alexandre Valentin Jamet, **Georgios Vavouliotis**, Lluc Alvarez, Daniel A. Jiménez, Marc Casas, A Two Level Neural Approach Combining Off-Chip Prediction with Adaptive Prefetch Filtering (to appear). Proceedings of the 30th International Symposium on High-Performance Computer Architecture (HPCA), Edinburgh, March 2024.

[3] Maria Carpen-Amarie, **Georgios Vavouliotis**, Konstantinos Tovletoglou, Boris Grot, Rene Mueller, Concurrent GCs and Modern Java Workloads: A Cache Perspective. Proceedings of the 2023 ACM SIGPLAN International Symposium on Memory Management (ISMM), Orlando, June 2023. [Best Paper Award]

[4] **Georgios Vavouliotis**, Gino Chancon, Lluc Alvarez, Paul V. Gratz, Daniel A. Jiménez, Marc Casas, Page Size Aware Cache Prefetching. Proceedings of the 55th IEEE/ACM International Symposium on Microarchitecture (MICRO), Chicago, Oct 2022.

[5] **Georgios Vavouliotis**, Lluc Alvarez, Boris Grot, Daniel A. Jiménez, Marc Casas, *Morrigan: A Composite Instruction TLB Prefetcher*. Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture (MICRO), Virtual, Oct 2021.

[6] **Georgios Vavouliotis**, Lluc Alvarez, Vasileios Karakostas, Konstantinos Nikas, Nectarios Koziris, Daniel A. Jiménez, Marc Casas, *Exploiting Page Table Locality for Agile TLB Prefetching*. Proceedings of the 48th International Symposium on Computer Architecture (ISCA), Virtual, June 2021. Also presented as a *Poster* at the 49th International Symposium on Computer Architecture (ISCA), New York, June 2022.

Peer-Reviewed Journal/Workshop Publications and Posters

[1] **Georgios Vavouliotis**, Gino Chancon, Lluc Alvarez, Paul V. Gratz, Daniel A. Jiménez, Marc Casas, *Leveraging Page Size Information to Enhance Data Cache Prefetching*. Poster at the 2021 ACM Summer School on HPC Computer Architectures for AI and Dedicated Applications, Virtual, Aug 2021. [Best Poster Award]

[2] **Georgios Vavouliotis**, Lluc Alvarez, Marc Casas, *Pushing the envelope on free TLB prefetching*. Proceedings of the 8th BSC Doctoral Symposium, Virtual, May 2021.

[3] **Georgios Vavouliotis**, *Cost-Effective Instruction TLB Prefetching*. Second Young Architect Workshop (YArch 2020). In conjunction with The 25th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Virtual, March 2020.

Dissertations

[1] **Georgios Vavouliotis** *"Advanced Hardware Prefetching in Virtual Memory Systems"*. Book of my Doctoral dissertation.

> **Thesis Statement:** *Hardware TLB prefetching can reduce the address translation overheads posed with applications with large data and code footprints while exploiting address translation metadata available at the microarchitecture and runtime levels can improve the performance of cache prefetchers.*

[2] **Georgios Vavouliotis**, Goumas Georgios, *"Performance Analysis of TLB Prefetching Mechanisms"*. Book of my Diploma thesis (in Greek).

Invited Talks

Advanced Hardware Prefetching in Virtual Memory Systems — **Athens**
6th Computing Systems Research Day @ CSLab — *Jan 2023*

Page Size Aware Cache Prefetching — **Chicago**
55th IEEE/ACM International Symposium on Microarchitecture (MICRO) — *Oct 2022*

Morrigan: A Composite Instruction TLB Prefetcher — **Zurich**
Huawei Zurich Research Center — *Dec 2021*

Morrigan: A Composite Instruction TLB Prefetcher — **Virtual**
54th IEEE/ACM International Symposium on Microarchitecture (MICRO) — *Oct 2021*

Leveraging Page Size Information to Enhance Data Cache Prefetching — **Virtual**
ACM School on HPC Computer Architectures for AI and Dedicated Applications — *Aug 2021*

Exploiting Page Table Locality for Agile TLB Prefetching — **Virtual**
48th International Symposium on Computer Architecture (ISCA) — *June 2021*

Pushing the Envelope on Free TLB Prefetching — **Virtual**
8th BSC Doctoral Symposium — *May 2021*

Professional Activities - Leadership & Service

ASPLOS'25 — **Rotterdam**
Program Committee (PC) member — *2024-2025*

ISCA'24 — **Buenos Aires**
Industry Track Program Committee (PC) member — *2023-2024*

Euro-Par'24 — **Madrid**
Program Committee (PC) member — *2023-2024*

HPCA'24 — **Edinburgh**
Artifact Evaluation Committee member — *2023-2024*

ISCA'24 — **Buenos Aires**
Website Co-Chair — *2023-2024*

Technical Reviewer for Conferences and Journals

- **International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'25)**
- **International Symposium on Computer Architecture (ISCA'24)**
- **European Conference on Parallel and Distributed Computing (Euro-Par'24)**
- **International Symposium on High-Performance Computer Architecture (HPCA'24)-Artifact Evaluation**
- **Journal of Parallel and Distributed Computing (JPDC'23)**
- **IEEE Access 2023**
- **ACM Transactions on Architecture and Code Optimization (TACO'23)**
- **IEEE Supercomputing Conference (SC'21)**
- **IEEE Transactions on Computers (2021)**
- **ACM International Conference on Computing Frontiers (CF'21)**

Teaching Experience

Private Tutor — **Athens**
C programming, Computer Architecture, Automatic Control for undergraduate students — *2013–2018*

Lab Assistant at National Technical University of Athens (NTUA) — **Athens**
C programming — *2013-2017*

Selected Press

TCuArch Interview — **youtube**
What attracted you to research computer architecture and systems? — *Dec 2022*

Languages

○ Greek (Native)   ○ English   ○ Italian (Beginner)   ○ Spanish (Beginner)